Stratix V Device Handbook

Volume 1: Overview and Datasheet

101 Innovation Drive
San Jose, CA 95134
www.altera.com

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Contents

Additional Information

Chapter Revision Dates

The chapters in this document, *Stratix V Device Handbook Volume 1*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1. Stratix V Device Family Overview
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Chapter 2. DC and Switching Characteristics for Stratix V Devices
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1. Stratix V Device Family Overview

SV51001-2.2

This chapter provides an overview of the Stratix® V devices and their features. Many of these devices and features are enabled in the Quartus® II software version 11.1. The remaining devices and features will be enabled in future versions of the Quartus II software.

To find out more about the upcoming Stratix V devices and features, refer to the *Stratix V Upcoming Device Features* document.

Altera's 28-nm Stratix V FPGAs include innovations such as an enhanced core architecture, integrated transceivers up to 28.05 gigabits per second (Gbps), and a unique array of integrated hard intellectual property (IP) blocks. With these innovations, Stratix V FPGAs deliver a new class of application-targeted devices optimized for:

- Bandwidth-centric applications and protocols, including PCI Express® (PCIe®) Gen3
- Data-intensive applications for 40G/100G and beyond
- High-performance, high-precision digital signal processing (DSP) applications

Stratix V devices are available in four variants (GT, GX, GS, and E), each targeted for a different set of applications. For higher volume production, you can prototype with Stratix V FPGAs and use the low-risk, low-cost path to HardCopy® V ASICs.

Stratix V Family Variants

Stratix V GT devices, with both 28.05-Gbps and 12.5-Gbps transceivers, are optimized for applications that require ultra-high bandwidth and performance in areas such as 40G/100G/400G optical communications systems and optical test systems. 28.05-Gbps and 12.5-Gbps transceivers are also known as GT and GX channels, respectively.

Stratix V GX devices offer up to 66 integrated 14.1-Gbps transceivers supporting backplanes and optical modules. These devices are optimized for high-performance, high-bandwidth applications such as 40G/100G optical transport, packet processing, and traffic management found in wireline, military communications, and network test equipment markets.

Stratix V GS devices have an abundance of variable precision DSP blocks, supporting up to 3,926 18x18 or 1,963 27x27 multipliers. In addition, Stratix V GS devices offer integrated 14.1-Gbps transceivers, which support backplanes and optical modules. These devices are optimized for transceiver-based DSP-centric applications found in wireline, military, broadcast, and high-performance computing markets.

Stratix V E devices offer the highest logic density within the Stratix V family with nearly one million logic elements (LEs) in the largest device. These devices are optimized for applications such as ASIC and system emulation, diagnostic imaging, and instrumentation.

Common to all Stratix V family variants are a rich set of high-performance building blocks, including a redesigned adaptive logic module (ALM), 20 Kbit (M20K) embedded memory blocks, variable precision DSP blocks, and fractional phase-locked loops (PLLs). All of these building blocks are interconnected by Altera's superior multi-track routing architecture and comprehensive fabric clocking network.

Also common to Stratix V devices is the new Embedded HardCopy Block, which is a customizable hard IP block that leverages Altera's unique HardCopy ASIC capabilities. The Embedded HardCopy Block in Stratix V FPGAs is used to harden IP instantiation of PCIe Gen3, Gen2, and Gen1 (Gen3/2/1).

Stratix V Features Summary

- Technology
  - 28-nm TSMC process technology
  - 0.85-V core voltage
- Low-power serial transceivers
  - 28.05-Gbps transceivers on Stratix V GT devices
  - Electronic dispersion compensation (EDC) for XFP, SFP+, QSFP, CFP optical module support
  - Adaptive linear and decision feedback equalization
  - 600-Megabits per second (Mbps) to 14.1-Gbps backplane capability
  - Transmit pre-emphasis and de-emphasis
  - Dynamic reconfiguration of individual channels
  - On-chip instrumentation (EyeQ non-intrusive data eye monitoring)
- General-purpose I/Os (GPIOs)
  - 1.4-Gbps LVDS
  - 1,066-MHz external memory interface
  - On-chip termination (OCT)
  - 1.2-V to 3.3-V interfacing for all Stratix V devices
- Embedded HardCopy Block
  - PCIe Gen3/2/1 complete protocol stack, x1/x2/x4/x8 end point and root port
- Embedded transceiver hard IP
  - Interlaken physical coding sublayer (PCS)
  - Gigabit Ethernet (GbE) and XAUI PCS
  - 10G Ethernet PCS
  - Serial RapidIO® (SRIO) PCS
  - Common Public Radio Interface (CPRI) PCS
  - Gigabit Passive Optical Networking (GPON) PCS
- Power Management
  - Programmable Power Technology
  - Quartus II integrated PowerPlay Power Analysis
- High-performance core fabric
  - Enhanced ALM with four registers
  - Improved routing architecture reduces congestion and improves compile times
- Embedded memory blocks
  - M20K: 20-Kbit with hard error correction code (ECC)
  - MLAB: 640-bit
- Variable precision DSP blocks
  - Up to 500 MHz performance
  - Natively support signal processing with precision ranging from 9x9 up to 54x54
  - New native 27x27 multiply mode
  - 64-bit accumulator and cascade for systolic finite impulse responses (FIRs)
  - Embedded internal coefficient memory
  - Pre-adder/subtractor improves efficiency
  - Increased number of outputs allows more independent multipliers
- Fractional PLLs
  - Fractional mode with third-order delta-sigma modulation
  - Integer mode
  - Precision clock synthesis, clock delay compensation, and zero delay buffer (ZDB)
- Clock networks
  - 717-MHz fabric clocking
  - Global, quadrant, and peripheral clock networks
  - Unused clock networks can be powered down to reduce dynamic power
- Device Configuration
  - Serial and parallel flash interface
  - Enhanced advanced encryption standard (AES) design security features
  - Tamper protection
  - Partial and dynamic reconfiguration
  - Configuration via Protocol (CvP)
- High-performance packaging
  - Multiple device densities with identical package footprints enables seamless migration between different FPGA densities
  - FBGA packaging with on-package decoupling capacitors
  - Lead and RoHS-compliant lead-free options
- HardCopy V migration

Stratix V Family Plan

Table 1–1 lists the Stratix V GT device features.

Table 1–1. Stratix V GT Device Features

Feature	5SGTC5	5SGTC7
Logic Elements (K)	425	622
Registers (K)	642	939
28.05/12.5-Gbps Transceivers	4/32	4/32
PCIe hard IP Blocks	1	1
Fractional PLLs	28	28
M20K Memory Blocks	2,304	2,560
M20K Memory (MBits)	45	50
Variable Precision Multipliers (18x18)	512	512
Variable Precision Multipliers (27x27)	256	256
DDR3 SDRAM x72 DIMM Interfaces	4	4
User I/Os, Full-Duplex LVDS, 28.05/12.5-Gbps Transceivers		
Package *(1), (2), (3)*	**5SGTC5**	**5SGTC7**
KF40-F1517 *(4)*	600, 150, 36	600, 150, 36

Notes to Table 1–1:

(1) Packages are flipchip ball grid array (1.0-mm pitch).

(2) Each package row offers pin migration (common board footprint) for all devices in the row.

(3) For full package details, refer to *Package Information Datasheet for Altera Devices*.

(4) Migration between select Stratix V GT devices and Stratix V GX devices is available. For more information, refer to Table 1–5 on page 1–9.

Table 1–2 lists the Stratix V GX device features.

Table 1–2. Stratix V GX Device Features (Part 1 of 2)

Features	5SGXA3	5SGXA4	5SGXA5	5SGXA7	5SGXA9	5SGXAB	5SGXB5	5SGXB6
Logic Elements (K)	340	420	490	622	840	952	490	597
Registers (K)	513	634	740	939	1,268	1,437	740	902
14.1-Gbps Transceivers	12, 24, or 36	24 or 36	24, 36, or 48	24, 36, or 48	36 or 48	36 or 48	66	66
PCIe hard IP Blocks	1 or 2	1 or 2	1, 2, or 4	1, 2, or 4	1, 2, or 4	1, 2, or 4	1 or 4	1 or 4
Fractional PLLs	20 (1)	24	28	28	28	28	24	24
M20K Memory Blocks	957	1,900	2,304	2,560	2,640	2,640	2,100	2,660
M20K Memory (MBits)	19	37	45	50	52	52	41	52
Variable Precision Multipliers (18x18)	512	512	512	512	704	704	798	798
Variable Precision Multipliers (27x27)	256	256	256	256	352	352	399	399
DDR3 SDRAM x72 DIMM Interfaces	4	4	6	6	6	6	4	4
User I/Os, Full-Duplex LVDS, 14.1-Gbps Transceivers								
Package (2), (3), (4), (5)	**5SGXA3**	**5SGXA4**	**5SGXA5**	**5SGXA7**	**5SGXA9**	**5SGXAB**	**5SGXB5**	**5SGXB6**
EH29-H780	360, 90, 12^{H}	—	—	—	—	—	—	—
HF35-F1152 (6)	432, 108, 24	552, 138, 24	552, 138, 24	552, 138, 24	—	—	—	—
KF35-F1152	432, 108, 36	432, 108, 36	432, 108, 36	432, 108, 36	—	—	—	—
KF40-F1517 / KH40-H1517 (6)	696, 174, 36	696, 174, 36	696, 174, 36	696, 174, 36	696, 174, 36^{H}	696, 174, 36^{H}	—	—
NF40-F1517 (7)	—	—	600, 150, 48	600, 150, 48	—	—	—	—
RF40-F1517	—	—	—	—	—	—	432, 108, 66	432, 108, 66
RF43-F1760	—	—	—	—	—	—	600, 150, 66	600, 150, 66

Table 1–2. Stratix V GX Device Features (Part 2 of 2)

Features	5SGXA3	5SGXA4	5SGXA5	5SGXA7	5SGXA9	5SGXAB	5SGXB5	5SGXB6
NF45-F1932 *(6)*	—	—	840, 210, 48	840, 210, 48	840, 210, 48	840, 210, 48	—	—

Notes to Table 1–2:

(1) The F1517 package contains 24 PLLs. The other packages with this device contain 20 PLLs.
(2) Packages are flipchip ball grid array (1.0-mm pitch).
(3) LVDS counts are full duplex channels. Each full duplex channel is one transmitter (TX) pair plus one receiver (RX) pair.
(4) Each package row offers pin migration (common circuit board footprint) for all devices in the row.
(5) ^{H} indicates a Hybrid package.
(6) Migration between select Stratix V GX devices and Stratix V GS devices is available. For more information, refer to Table 1–5 on page 1–9.
(7) Migration between select Stratix V GX devices and Stratix V GT devices is available. For more information, refer to Table 1–5 on page 1–9.

Table 1–3 lists the Stratix V GS device features.

Table 1–3. Stratix V GS Device Features

Features	5SGSD3	5SGSD4	5SGSD5	5SGSD6	5SGSD8
Logic Elements (K)	236	360	457	583	695
Registers (K)	356	543	690	880	1,050
14.1-Gbps transceivers	12 or 24	12, 24, or 36	24 or 36	36 or 48	36 or 48
PCIe hard IP blocks	1	1	1	1, 2, or 4	1, 2, or 4
Fractional PLLs	20	20 (1)	24	28	28
M20K Memory Blocks	688	957	2,014	2,320	2,567
M20K Memory (MBits)	13	19	39	45	50
Variable Precision Multipliers (18x18)	1,200	2,088	3,180	3,550	3,926
Variable Precision Multipliers (27x27)	600	1,044	1,590	1,775	1,963
DDR3 SDRAM x72 DIMM Interfaces	2	4	4	6	6
User I/Os, Full-Duplex LVDS, 14.1-Gbps Transceivers					
Package (2), (3), (4), (5)	**5SGSD3**	**5SGSD4**	**5SGSD5**	**5SGSD6**	**5SGSD8**
EH29-H780	360, 90, 12^{H}	360, 90, 12^{H}	—	—	—
HF35-F1152 (6)	432, 108, 24	432, 108, 24	552, 138, 24	—	—
KF40-F1517 (6)	—	696, 174, 36	696, 174, 36	696, 174, 36	696, 174, 36
NF45-F1932 (6)	—	—	—	840, 210, 48	840, 210, 48

Notes to Table 1–3:

(1) The F1517 package contains 24 PLLs. The other packages with this device contain 20 PLLs.
(2) Packages are flipchip ball grid array (1.0-mm pitch).
(3) LVDS counts are full duplex channels. Each full duplex channel is one TX pair plus one RX pair.
(4) Each package row offers pin migration (common circuit board footprint) for all devices in the row.
(5) ^{H} indicates a Hybrid package.
(6) Migration between select Stratix V GS devices and Stratix V GX devices is available. For more information, refer to Table 1–5 on page 1–9.

Table 1–4 lists the Stratix V E device features.

Table 1–4. Stratix V E Device Features

Features	5SEE9	5SEEB
Logic Elements (K)	840	952
Registers (K)	1,268	1,437
Fractional PLLs	28	28
M20K Memory Blocks	2,640	2,640
M20K Memory (MBits)	52	52
Variable Precision Multipliers (18x18)	704	704
Variable Precision Multipliers (27x27)	352	352
DDR3 SDRAM x72 DIMM Interfaces	6	6
User I/Os, Full-Duplex LVDS		
Package *(1), (2), (3), (4)*	**5SEE9**	**5SEEB**
H40-H1517	696, 174[H]	696, 174[H]
F45-F1932	840, 210	840, 210

Notes to Table 1–4:

(1) Packages are flipchip ball grid array (1.0-mm pitch).
(2) LVDS counts are full duplex channels. Each full duplex channel is one TX pair plus one RX pair.
(3) Each package row offers pin migration (common circuit board footprint) for all devices in the row.
(4) [H] indicates a Hybrid package.

Each row in Table 1–5 lists which devices allow migration.

Table 1–5. Device Migration List Across All Stratix V Device Variants *(1)*

Package	Stratix V GX								Stratix V GT		Stratix V GS					Stratix V E	
	A3	A4	A5	A7	A9	AB	B5	B6	C5	C7	D3	D4	D5	D6	D8	E9	EB
EH29-H780	✓										✓	✓					
HF35-F1152 *(2)*	✓	✓	✓	✓							✓	✓	✓				
KF35-F1152	✓	✓	✓	✓													
KF40-F1517 / KH40-H1517	✓	✓	✓	✓	✓	✓						✓	✓	✓	✓		
NF40 / KF40-F1517 *(3)*			✓	✓					✓	✓							
RF40-F1517							✓	✓									
H40-H1517																✓	✓
RF43-F1760							✓	✓									
NF45-F1932			✓	✓	✓	✓								✓	✓		
F45-F1932																✓	✓

Notes to Table 1–5:

(1) All devices in a given row allow migration.

(2) All devices in this row are in the HF35 package and have twenty-four 14.1-Gbps transceivers.

(3) The 5SGTC5/7 devices in the KF40 package have four 28.05-Gbps transceivers and thirty-two 12.5-Gbps transceivers. Other devices in this row are in the NF40 package and have forty-eight 14.1-Gbps transceivers.

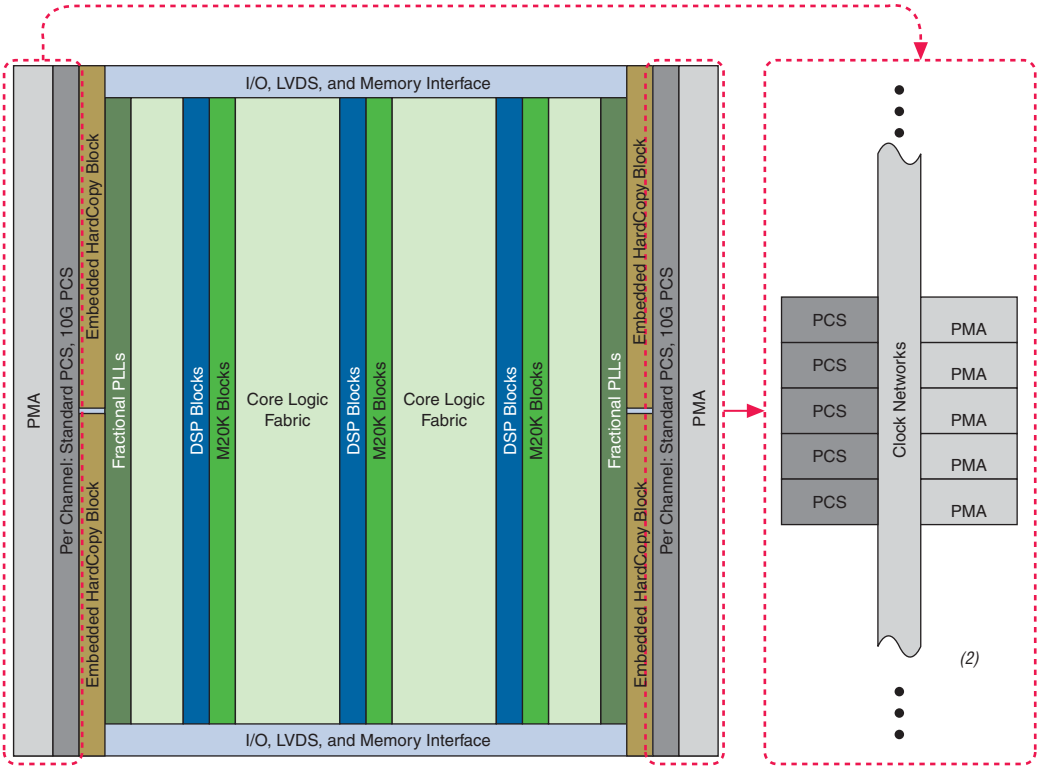
Low-Power Serial Transceivers

Stratix V FPGAs deliver the industry's most flexible transceivers with the highest bandwidth from 600 Mbps to 28.05 Gbps, low bit error ratio (BER), and low power. Stratix V transceivers have many enhancements to improve flexibility and robustness. These enhancements include robust analog receive clock and data recovery (CDR), advanced pre-emphasis, and equalization. In addition, all transceivers are identical with the full featured embedded PCS hard IP to simplify the design, lower the power, and save valuable core resources.

Stratix V transceivers are compliant with a wide range of standard protocols and data rates and are equipped with a variety of signal-conditioning features to support backplane, optical module, and chip-to-chip applications.

Stratix V transceivers are located on the left and right sides of the device, as shown in Figure 1–1. The transceivers are isolated from the rest of the chip to prevent core and I/O noise from coupling into the transceivers, thereby ensuring optimal signal integrity. The transceiver channels consist of the physical medium attachment (PMA), PCS, and high-speed clock networks. You can also use the unused transceiver PMA channels as additional transmit PLLs. Table 1–6 lists the transceiver PMA features.

Figure 1–1. Stratix V GT, GX, and GS Device Chip View *(1)*



Notes to Figure 1–1:

(1) This figure represents a given variant of a Stratix V device with transceivers. Other variants may have a different floorplan than the one shown here.

(2) You can use the unused transceiver channels as additional transceiver transmit PLLs.

Table 1–6 lists the PMA features for the Stratix V transceivers.

Table 1–6. Transceiver PMA Features

Feature	Capability
Backplane support	10GBASE-R, 14.1 Gbps (Stratix V GX and GS devices), 12.5 Gbps (Stratix V GT devices)
Cable driving support	PCIe cable and eSATA applications
Optical module support with EDC	10G Form-factor Pluggable (XFP), Small Form-factor Pluggable (SFP+), Quad Small Form-factor Pluggable (QSFP), CXP, 100G Pluggable (CFP), 100G Form-factor Pluggable
Chip-to-chip support	28.05 Gbps and 12.5 Gbps (Stratix V GT devices) and 14.1 Gbps (Stratix V GX and GS devices)
Continuous Time Linear Equalization (CTLE)	Receiver 4-stage linear equalization to support high-attenuation channels
Decision Feedback Equalization (DFE)	Receiver 5-tap digital equalizer to minimize losses and crosstalk
Adaptive equalization (AEQ)	Adaptive engine to automatically adjust equalization to compensate for changes over time
PLL-based clock recovery	Superior jitter tolerance versus phase interpolation techniques
Programmable deserialization and word alignment	Flexible deserialization width and configurable word alignment patterns
Transmit equalization (pre-emphasis)	Transmit driver 4-tap pre-emphasis and de-emphasis for protocol compliance under lossy conditions
Ring and logic cell oscillator transmit PLLs	Choice of transmit PLLs per channel, optimized for specific protocols and applications
On-chip instrumentation (EyeQ data-eye monitor)	Allows non-intrusive on-chip monitoring of both width and height of the data eye
Dynamic reconfiguration	Allows reconfiguration of single channels without affecting operation of other channels
Protocol support	Compliance with over 50 industry standard protocols in the range of 600 Mbps to 28 Gbps

The Stratix V core logic connects to the PCS through an 8-, 10-, 16-, 20-, 32-, 40-, 64-, or 66-bit interface, depending on the transceiver data rate and protocol. Stratix V devices contain PCS hard IP to support PCIe Gen3/2/1, Interlaken, 10GE, XAUI, GbE, SRIO, CPRI, and GPON protocols. All other standard and proprietary protocols are supported through the transceiver PCS hard IP. Table 1–7 lists the transceiver PCS features.

Table 1–7. Transceiver PCS Features (Part 1 of 2)

Protocol	Data Rates (Gbps)	Transmit Data Path	Receiver Data Path
Custom PHY	0.6 to 8.5	Phase compensation FIFO, byte serializer, 8B/10B encoder, bit-slip, and channel bonding	Word aligner, de-skew FIFO, rate match FIFO, 8B/10B decoder, byte deserializer, and byte ordering
Custom 10G PHY	9.98 to 14.1	TX FIFO, gear box, and bit-slip	RX FIFO and gear box
x1, x4, x8 PCIe Gen1/2	2.5 and 5.0	Same as custom PHY plus PIPE 2.0 interface to core logic	Same as custom PHY plus PIPE 2.0 interface to core logic

Table 1–7. Transceiver PCS Features (Part 2 of 2)

Protocol	Data Rates (Gbps)	Transmit Data Path	Receiver Data Path
x1, x4, x8 PCIe Gen3	8	Phase compensation FIFO, encoder, scrambler, gear box, and bit slip	Block synchronization, rate match FIFO, decoder, de-scrambler, and phase compensation FIFO
10G Ethernet	10.3125	TX FIFO, 64/66 encoder, scrambler, and gear box	RX FIFO, 64/66 decoder, de-scrambler, block synchronization, and gear box
Interlaken	4.9 to 10.3125	TX FIFO, frame generator, CRC-32 generator, scrambler, disparity generator, and gear box	RX FIFO, frame generator, CRC-32 checker, frame decoder, descrambler, disparity checker, block synchronization, and gearbox
40GBASE-R Ethernet	4 x 10.3125	TX FIFO, 64/66 encoder, scrambler, alignment marker insertion, gearbox, and block striper	RX FIFO, 64/66 decoder, de-scrambler, lane reorder, deskew, alignment marker lock, block synchronization, gear box, and destripper
100GBASE-R Ethernet	10 x 10.3125		
OTN 40 and 100	(4 +1) x 11.3	TX FIFO, channel bonding, and byte serializer	RX FIFO, lane deskew, and byte de-serializer
	(10 +1) x 11.3		
GbE	1.25	Same as custom PHY plus GbE state machine	Same as custom PHY plus GbE state machine
XAUI	3.125 to 4.25	Same as custom PHY plus XAUI state machine for bonding four channels	Same as custom PHY plus XAUI state machine for re-aligning four channels
SRIO	1.25 to 6.25	Same as custom PHY plus SRIO V2.1 compliant x2 and x4 channel bonding	Same as custom PHY plus SRIO V2.1-compliant x2 and x4 deskew state machine
CPRI	0.6144 to 9.83	Same as custom PHY plus TX deterministic latency	Same as custom PHY plus RX deterministic latency
GPON	1.25, 2.5, and 10	Same as custom PHY	Same as custom PHY

PCIe Gen3/2/1 Hard IP (Embedded HardCopy Block)

Stratix V devices have PCIe hard IP designed for performance, ease-of-use, and increased functionality. The PCIe hard IP consists of the PCS, data link, and transaction layers. The PCIe hard IP supports Gen3/2/1 end point and root port up to x8 lane configurations.

The Stratix V PCIe hard IP operates independently from the core logic, which allows the PCIe link to wake up and complete link training in less than 100 ms while the Stratix V device completes loading the programming file for the rest of the FPGA. The PCIe hard IP also provides added functionality, which makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) or optional protocol extensions. In addition, the Stratix V device PCIe hard IP has improved end-to-end data path protection using ECC and enables device CvP.

In all Stratix V devices, the primary PCIe hard IP that supports CvP is always in the bottom left corner of the device (IOBANK_B0L) when looking at the top view of the die.

External Memory and GPIO

Each Stratix V I/O block has a hard FIFO that improves the resynchronization margin as data is transferred from memory to the FPGA. The hard FIFO also lowers PHY latency, resulting in higher random access performance. GPIOs include on-chip dynamic termination to reduce the number of external components and minimize reflections. On-package decoupling capacitors suppress noise on the power lines, which reduce noise coupling into the I/Os. Memory banks are isolated to prevent core noise from coupling to the output, thus reducing jitter and providing optimal signal integrity.

The external memory interface block also uses advanced calibration algorithms to compensate for process, voltage and temperature (PVT) variations in the FPGA and external memory components. The advanced algorithms ensure maximum bandwidth and a robust timing margin across all conditions. Stratix V devices also deliver a complete memory solution with the High Performance Memory Controller II (HPMC II) and UniPHY MegaCore® IP that simplify a design for today's advanced memory modules. Table 1–8 lists external memory interface block performance.

Table 1–8. External Memory Interface Performance *(1)*

Interface	Performance (MHz)
DDR3	1,066
DDR2	533
QDR II	350
QDR II+	550
RLDRAM II	533
RLDRAM III	800

Note to Table 1–8:

(1) The specifications listed in this table are performance targets. For a current achievable performance, use the External Memory Interface Spec Estimator.

Adaptive Logic Module

Stratix V devices use an improved ALM to implement logic functions more efficiently. The Stratix V ALM has eight inputs with a fracturable look-up table (LUT), two dedicated embedded adders, and four dedicated registers.

The Stratix V ALM has the following enhancements:

- Packs 6% more logic when compared with the ALM found in Stratix IV devices
- Implements select 7-input LUT-based functions, all 6-input logic functions, and two independent functions consisting of smaller LUT sizes (such as two independent 4-input LUTs) to optimize core usage
- Adds more registers (four registers per 8-input fracturable LUT). More registers allow Stratix V devices to maximize core performance at a higher core logic usage and provides easier timing closure for register-rich and heavily pipelined designs.

The Quartus II software leverages the Stratix V ALM logic structure to deliver the highest performance, optimal logic usage, and lowest compile times. The Quartus II software simplifies design re-use because it automatically maps legacy Stratix designs into the new Stratix V ALM architecture.

Clocking

The Stratix V device core clock network is designed to support 717-MHz fabric operations and 1,066-MHz and 1,600-Mbps external memory interfaces. The clock network architecture is based on Altera's proven global, quadrant, and peripheral clock structure, which is supported by dedicated clock input pins and fractional clock synthesis PLLs. The Quartus II software identifies all unused sections of the clock network and powers them down, which reduces power consumption.

Fractional PLL

Stratix V devices have up to 28 fractional PLLs that you can use to reduce both the number of oscillators required on the board and the clock pins used in the FPGA by synthesizing multiple clock frequencies from a single reference clock source. In addition, you can use the fractional PLLs for clock network delay compensation, zero delay buffering, and transmit clocking for transceivers. Fractional PLLs may be individually configured for integer mode or fractional mode with third-order delta-sigma modulation.

Embedded Memory

Stratix V devices contain two types of embedded memory blocks: MLAB (640-bit) and M20K (20-Kbit). MLAB blocks are ideal for wide and shallow memories. M20K blocks are useful for supporting larger memory configurations and include ECC. Both types operate at up to 600 MHz and are configurable to be a single- or dual-port RAM, FIFO, ROM, or shift register. These memory blocks are flexible and support a number of memory configurations, as shown in Table 1–9.

Table 1–9. Embedded Memory Block Configuration

MLAB (640 Bits)	M20K (20,480 Bits)
32x20 64x10	512x40 1Kx20 2Kx10 4Kx5 8Kx2 16Kx1

The Quartus II software simplifies design re-use by automatically mapping memory blocks from legacy Stratix devices into the Stratix V memory architecture.

Variable Precision DSP Block

Stratix V FPGAs feature the industry's first variable precision DSP block that you can configure to natively support signal processing with precision ranging from 9x9 to 36x36.

You can independently configure each DSP block at compile time as either a dual 18x18 multiply accumulate or a single 27x27 multiply accumulate. With a dedicated 64-bit cascade bus, you can cascade multiple variable precision DSP blocks to implement even higher precision DSP functions efficiently. Table 1–10 lists how different precision is accommodated within a DSP block or by using multiple blocks.

Table 1–10. Variable Precision DSP Block Configurations

Multiplier Size (bits)	DSP Block Resources	Expected Usage
9x9	1/3 of variable precision DSP block	Low precision fixed point
18x18	1/2 of variable precision DSP block	Medium precision fixed point
27x27	1 variable precision DSP block	High precision fixed or single precision floating point
36x36	2 variable precision DSP blocks	Very high precision fixed point

Complex multiplication is common in DSP algorithms. One of the most popular applications of complex multipliers is the fast Fourier transform (FFT) algorithm. This algorithm has the characteristic of increasing precision requirements on only one side of the multiplier. The variable precision DSP block is designed to support the FFT algorithm with a proportional increase in DSP resources with precision growth. Table 1–11 lists complex multiplication with variable precision DSP blocks.

Table 1–11. Complex Multiplication with Variable Precision DSP Blocks

Multiplier Size (bits)	DSP Block Resources	Expected Usage
18x18	2 variable precision DSP blocks	Resource optimized FFTs
18x25	3 variable precision DSP blocks	Accommodate bit growth through FFT stages
18x36	4 variable precision DSP blocks	Highest precision FFT stages
27x27	4 variable precision DSP blocks	Single precision floating point

Additionally, for FFT applications with high dynamic range requirements, only the Altera® FFT MegaCore offers an option of single precision floating point implementation, with the resource usage and performance similar to high-precision fixed point implementations.

Other new features include:

- 64-bit accumulator, the largest in the industry
- Hard pre-adder, available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic FIR filters
- Internal coefficient register banks
- Enhanced independent multiplier operation
- Efficient support for single- and double-precision floating point arithmetic
- Ability to infer all the DSP block modes through HDL code using the Quartus II design suite.

The variable precision DSP block is ideal for higher bit precision in high-performance DSP applications. At the same time, the variable precision DSP block can efficiently support the many existing 18-bit DSP applications, such as high definition video processing and remote radio heads. Stratix V FPGAs, with the variable precision DSP block architecture, are the only FPGA family that can efficiently support many different precision levels, up to and including floating point implementations. This flexibility results in increased system performance, reduced power consumption, and reduced architecture constraints on system algorithm designers.

Power Management

Stratix V devices leverage FPGA architectural features and process technology advancements to reduce total power consumption by as much as 30% when compared with Stratix IV devices at the same performance level.

Stratix V devices continue to provide programmable power technology, introduced in earlier generations of Stratix FPGA families. The Quartus II software PowerPlay feature identifies critical timing paths in a design and biases core logic in that path for high performance. The PowerPlay feature also identifies non-critical timing paths and biases core logic in that path for low power instead of high performance. PowerPlay automatically biases core logic to meet performance and optimize power consumption.

Additionally, Stratix V devices have a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings when compared with soft implementations. The list includes PCIe Gen1/Gen2/Gen3, Interlaken PCS, hard I/O FIFOs, and transceivers. Hard IP blocks consume up to 50% less power than equivalent soft implementations.

Stratix V transceivers are also designed for power efficiency. As a result, the transceiver channels consume 50% less power than the previous generation of Stratix FPGAs. The transceiver PMA consumes approximately 90 mW at 6.5 Gbps and 170 mW at 12.5 Gbps.

Incremental Compilation

The Quartus II software incremental compilation feature reduces compilation time by up to 70% and preserves performance to ease timing closure. Incremental compilation supports top-down, bottom-up, and team-based design flows. The incremental compilation feature facilitates modular hierarchical and team-based design flows where different designers compile their respective sections of a design in parallel. Furthermore, different designers or IP providers can develop and optimize different blocks of the design independently, which you can then import into the top-level project.

Enhanced Configuration and CvP

Stratix V device configuration is enhanced for ease-of-use, speed, and cost. Stratix V devices support a new 4-bit bus active serial mode (ASx4). ASx4 supports up to a 400-Mbps data rate using small low-cost quad interface Flash devices. ASx4 mode is easy to use and offers an ideal balance between cost and speed. Finally, the fast passive parallel (FPP) interface is enhanced to support 8-, 16-, and 32-bit data widths to meet a wide range of performance and cost goals.

You can configure Stratix V FPGAs using CvP with PCIe. CvP with PCIe separates the configuration process into two parts: the PCIe hard IP and periphery and the core logic fabric. CvP uses a much smaller amount of external memory (flash or ROM) because CvP only has to store the configuration file for the PCIe hard IP and periphery. Also, the 100-ms power-up to active time (for PCIe) is much easier to

achieve when only the PCIe hard IP and periphery are loaded. After the PCIe hard IP and periphery are loaded and the root port is booted up, application software running on the root port can send the configuration file for the FPGA fabric across the PCIe link where it is loaded into the FPGA. The FPGA is then fully configured and functional.

Table 1–12 lists the available configuration modes for Stratix V devices.

Table 1–12. Configuration Modes for Stratix V Devices

Mode	Fast or Slow POR	Compression	Encryption	Remote Update	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps)
Active Serial (AS)	✓	✓	✓	✓	1, 4	100	400
Passive Serial (PS)	✓	✓	✓	—	1	125	125
Fast Passive Parallel (FPP)	✓	✓	✓	*(1)*	8, 16, 32	125	3,000
CvP	—	—	✓	✓	1, 2, 4, 8	—	3,000
Partial Reconfiguration	—	—	✓	✓	16	125	2,000
JTAG	—	—	—	—	1	33	33

Note to Table 1–12:

(1) Remote update support with the Parallel Flash Loader.

Partial Reconfiguration

Partial reconfiguration allows you to reconfigure part of the FPGA while other sections continue to operate. This capability is required in systems where uptime is critical because partial reconfiguration allows you to make updates or adjust functionality without disrupting services. While lowering power and cost, partial reconfiguration also increases the effective logic density by removing the necessity to place the FPGA functions that do not operate simultaneously. Instead, you can store these functions in external memory and load them as required. This reduces the size of the FPGA by allowing multiple applications on a single FPGA, saving board space and reducing power.

Up to now, partial reconfiguration solutions have been time-intensive tasks that required you to know all of the intricate FPGA architecture details. Altera simplifies the partial reconfiguration process by building the capability on top of the proven incremental compilation design flow in its Quartus II design software.

Partial reconfiguration is supported through the following configuration options:

- Partial reconfiguration through the FPP x16 I/O interface
- CvP
- Soft internal core, such as the Nios® II processor.

Automatic Single Event Upset (SEU) Error Detection and Correction

Stratix V devices offer new SEU error detection and correction circuitry that is robust and easy to use. The correction circuitry includes protection for configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running cyclical redundancy check (CRC) error detection circuit with integrated ECC that automatically corrects one or two errors and detects higher order multi-bit errors. When more than two errors occur, correction is available through a core programming file reload that provides a complete design refresh while the FPGA continues to operate.

Furthermore, the physical layout of the FPGA is optimized to make the majority of multi-bit upsets appear as independent single- or double-bit errors, which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection in Stratix V devices, user memories include integrated ECC circuitry and are layout-optimized to enable error detection of 12-bit errors and correction for 8-bit errors.

HardCopy V Devices

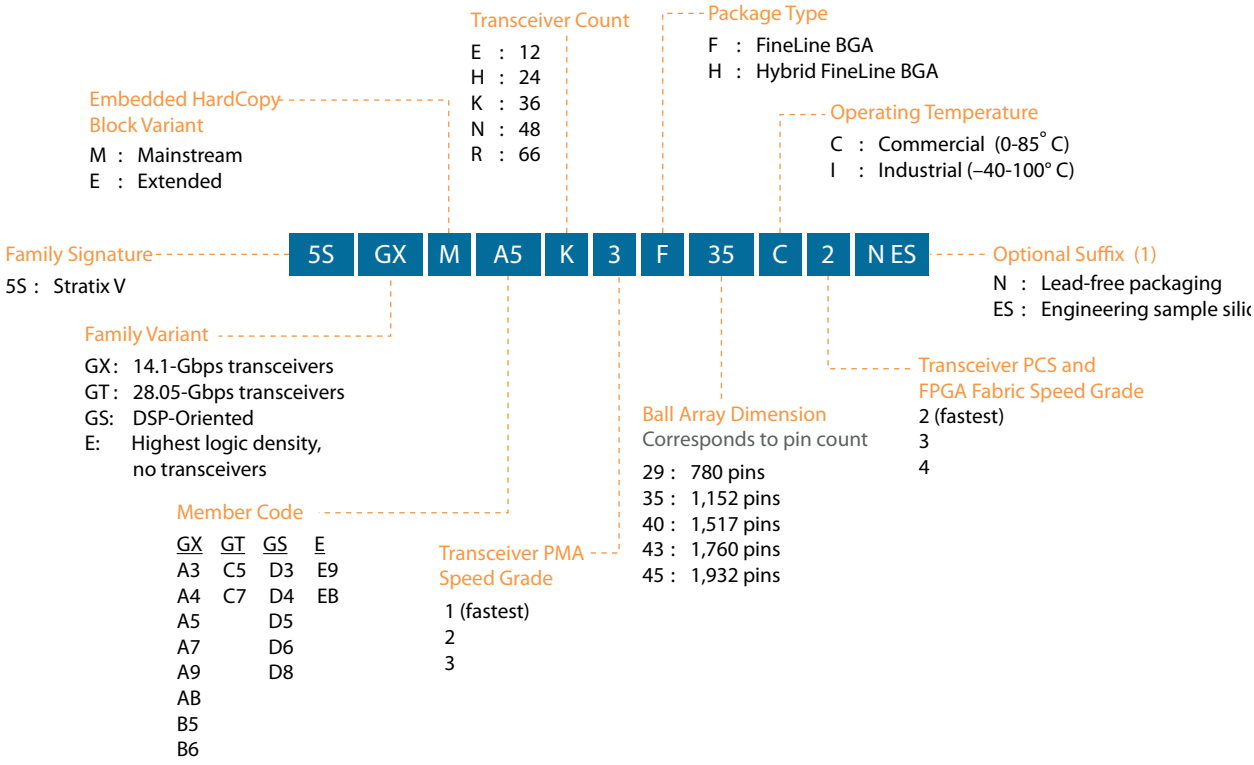
HardCopy V ASICs offer the lowest risk and lowest total cost in ASIC designs with embedded high-speed transceivers. You can prototype and debug with Stratix V FPGAs, then use HardCopy V ASICs for volume production. The proven turnkey process creates a functionally equivalent HardCopy V ASIC with or without embedded transceivers to meet all timing constraints in as little as 12 weeks.

The powerful combination of Stratix V FPGAs and HardCopy V ASICs can help you meet your design requirements. Whether you plan for ASIC production and require the lowest-risk, lowest-cost path from specification to production or require a cost reduction path for your FPGA-based systems, Altera provides the optimal solution for power, performance, and device bandwidth.

Ordering Information

This section describes ordering information for Stratix V GT, GX, GS, and E devices. Figure 1–2 shows the ordering codes for Stratix V devices.

Figure 1–2. Ordering Information for Stratix V Devices



Note to Figure 1–2:

(1) You can select one or both of these options, or you can ignore these options.

Revision History

Table 1–13 lists the revision history for this chapter.

Table 1–13. Revision History

Date	Version	Changes Made
December 2011	2.2	Updated Table 1–2 and Table 1–3.
November 2011	2.1	■ Changed Stratix V GT transceiver speed from 28 Gbps to 28.05 Gbps. ■ Updated Figure 1–2.
November 2011	2.0	■ Revised Figure 1–2. ■ Updated Table 1-5. ■ Minor text edits.
September 2011	1.10	Updated Table 1–2, Table 1–3, and Table 1–4.
September 2011	1.9	■ Updated Table 1–1, Table 1–2, Table 1–3, Table 1–4, and Table 1–5. ■ Updated Figure 1–2. ■ Minor text edits.
June 2011	1.8	Changed 800 MHz to 1,066 MHz for DDR3 in Table 1–8 and in text.
May 2011	1.7	■ For Stratix V GT devices, changed 14.1 Gbps to 12.5 Gbps. ■ Changed Configuration via PCIe to Configuration via Protocol ■ Updated Table 1–1, Table 1–2, Table 1–3, Table 1–4, Table 1–5, and Table 1–6. ■ Chapter moved to Volume 1.
January 2011	1.6	■ Added Stratix V GS information. ■ Updated tables listing device features. ■ Added device migration information. ■ Updated 12.5-Gbps transceivers to 14.1-Gbps transceivers
December 2010	1.5	Updated Table 1-1.
December 2010	1.4	■ Updated Table 1-1. ■ Updated Figure 1-2. ■ Converted to the new template. ■ Minor text edits.
July 2010	1.3	Updated Table 1–5
July 2010	1.2	■ Updated “Features Summary” on page 1–2 ■ Updated resource counts in Table 1–1 and Table 1–2 ■ Removed “Interlaken PCS Hard IP” and “10G Ethernet Hard IP” ■ Added “40G and 100G Ethernet Hard IP (Embedded HardCopy Block)” on page 1–7 ■ Added information about Configuration via PCIe ■ Added “Partial Reconfiguration” on page 1–12 ■ Added “Ordering Information” on page 1–14
May 2010	1.1	Updated part numbers in Table 1–1 and Table 1–2
April 2010	1.0	Initial release

2. DC and Switching Characteristics for Stratix V Devices

SV53001-2.2

This chapter covers the electrical and switching characteristics for Stratix® V devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This chapter also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

For information regarding the densities and packages of devices in the Stratix V family, refer to the *Stratix V Device Family Overview* chapter.

Electrical Characteristics

The following sections describe the electrical characteristics of Stratix V devices.

Operating Conditions

When you use Stratix V devices, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Stratix V devices, you must consider the operating requirements described in this chapter.

Stratix V devices are offered in commercial and industrial grades. Commercial devices are offered in –2 (fastest), –3, and –4 speed grades. Industrial devices are offered in –3 and –4 speed grades.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Stratix V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

CAUTION

Conditions other than those listed in Table 2–1 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 2–1. Absolute Maximum Ratings for Stratix V Devices—Preliminary (Part 1 of 2)

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Power supply for core voltage and periphery circuitry	–0.5	1.35	V
V_{CCPT}	Power supply for programmable power technology	–0.5	1.8	V
V_{CCPGM}	Power supply for configuration pins	–0.5	3.75	V
V_{CC_AUX}	Auxiliary supply for the programmable power technology	–0.5	3.75	V

Table 2–1. Absolute Maximum Ratings for Stratix V Devices—Preliminary (Part 2 of 2)

Symbol	Description	Minimum	Maximum	Unit
V_{CCBAT}	Battery back-up power supply for design security volatile key register	–0.5	3.75	V
V_{CCPD}	I/O pre-driver power supply	–0.5	3.75	V
V_{CCIO}	I/O power supply	–0.5	3.9	V
V_{CCD_FPLL}	PLL digital power supply	–0.5	3.75	V
V_{CCA_FPLL}	PLL analog power supply	–0.5	3.75	V
V_I	DC input voltage	–0.5	4.0	V
I_{OUT}	DC output current per pin	–25	40	mA
T_J	Operating junction temperature	–55	125	°C
T_{STG}	Storage temperature (No bias)	–65	150	°C

Table 2–2 lists the absolute conditions for the transceiver power supply for Stratix V GX, GS, and GT devices.

Table 2–2. Transceiver Power Supply Absolute Conditions for Stratix V GX, GS, and GT Devices

Symbol	Description	Devices	Minimum	Maximum	Unit
V_{CCA_GXBL}	Transceiver channel PLL power supply (left side)	GX, GS, GT	–0.5	3.75	V
V_{CCA_GXBR}	Transceiver channel PLL power supply (right side)	GX, GS	–0.5	3.75	V
V_{CCA_GTBR}	Transceiver channel PLL power supply (right side)	GT	–0.5	3.75	V
V_{CCHIP_L}	Transceiver hard IP power supply (left side)	GX, GS, GT	–0.5	1.35	V
V_{CCHIP_R}	Transceiver hard IP power supply (right side)	GX, GS, GT	–0.5	1.35	V
V_{CCHSSI_L}	Transceiver PCS power supply (left side)	GX, GS, GT	–0.5	1.35	V
V_{CCHSSI_R}	Transceiver PCS power supply (right side)	GX, GS, GT	–0.5	1.35	V
V_{CCR_GXBL}	Receiver analog power supply (left side)	GX, GS, GT	–0.5	1.35	V
V_{CCR_GXBR}	Receiver analog power supply (right side)	GX, GS, GT	–0.5	1.35	V
V_{CCR_GTBR}	Receiver analog power supply for GT channels (right side)	GT	–0.5	1.35	V
V_{CCT_GXBL}	Transmitter analog power supply (left side)	GX, GS, GT	–0.5	1.35	V
V_{CCT_GXBR}	Transmitter analog power supply (right side)	GX, GS, GT	–0.5	1.35	V
V_{CCT_GTBR}	Transmitter analog power supply for GT channels (right side)	GT	–0.5	1.35	V
V_{CCL_GTBR}	Transmitter clock network power supply (right side)	GT	–0.5	1.35	V
V_{CCH_GXBL}	Transmitter output buffer power supply (left side)	GX, GS, GT	–0.5	1.8	V
V_{CCH_GXBR}	Transmitter output buffer power supply (right side)	GX, GS, GT	–0.5	1.8	V

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 2–3 and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 2–3 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~5% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to half a year.

Table 2–3. Maximum Allowed Overshoot During Transitions—Preliminary

Symbol	Description	Condition (V)	Overshoot Duration as % @ T_J = 100°C	Unit
Vi (AC)	AC input voltage	3.8	100	%
		3.85	64	%
		3.9	36	%
		3.95	21	%
		4	12	%
		4.05	7	%
		4.1	4	%
		4.15	2	%
		4.2	1	%

Recommended Operating Conditions

This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 2–4 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 2–4. Recommended Operating Conditions for Stratix V Devices—Preliminary

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC}	Core voltage and periphery circuitry power supply	—	0.82	0.85	0.88	V
V_{CCPT}	Power supply for programmable power technology	—	1.45	1.50	1.55	V
V_{CC_AUX}	Auxiliary supply for the programmable power technology	—	2.375	2.5	2.625	V
V_{CCPD} (1)	I/O pre-driver (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O pre-driver (2.5 V) power supply	—	2.375	2.5	2.625	V
V_{CCIO}	I/O buffers (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply	—	1.283	1.35	1.45	V
	I/O buffers (1.25 V) power supply	—	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V
V_{CCPGM}	Configuration pins (3.0 V) power supply	—	2.85	3.0	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
V_{CCA_FPLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V_{CCD_FPLL}	PLL digital voltage regulator power supply	—	1.45	1.5	1.55	V
V_{CCBAT} (2)	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V
V_I	DC input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	–40	—	100	°C
t_{RAMP}	Power supply ramp time	Standard POR	200 µs	—	100 ms	—
		Fast POR	200 µs	—	4 ms	—

Notes to Table 2–4:

(1) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V.

(2) If you do not use the design security feature in Stratix V devices, connect V_{CCBAT} to a 2.5- or 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors V_{CCBAT}. Stratix V devices will not exit POR if V_{CCBAT} stays at logic low.

Table 2–5 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

Table 2–5. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices

Symbol	Description	Devices	Minimum	Typical	Maximum	Unit
V_{CCA_GXBL} (1)	Transceiver channel PLL power supply (left side)	GX, GS, GT	2.85, 2.375	3.0, 2.5	3.15, 2.625	V
V_{CCA_GXBR} (1)	Transceiver channel PLL power supply (right side)	GX, GS	2.85, 2.375	3.0, 2.5	3.15, 2.625	V
V_{CCA_GTBR}	Transceiver channel PLL power supply (right side)	GT	2.85	3.0	3.15	V
V_{CCHIP_L}	Transceiver hard IP power supply (left side)	GX, GS, GT	0.82	0.85	0.88	V
V_{CCHIP_R}	Transceiver hard IP power supply (right side)	GX, GS, GT	0.82	0.85	0.88	V
V_{CCHSSI_L}	Transceiver PCS power supply (left side)	GX, GS, GT	0.82	0.85	0.88	V
V_{CCHSSI_R}	Transceiver PCS power supply (right side)	GX, GS, GT	0.82	0.85	0.88	V
V_{CCR_GXBL} (2)	Receiver analog power supply (left side)	GX, GS, GT	0.82, 0.95	0.85, 1.0	0.88, 1.05	V
V_{CCR_GXBR} (2)	Receiver analog power supply (right side)	GX, GS, GT	0.82, 0.95	0.85, 1.0	0.88, 1.05	V
V_{CCR_GTBR}	Receiver analog power supply for GT channels (right side)	GT	0.95	1.0	1.05	V
V_{CCT_GXBL} (2)	Transmitter analog power supply (left side)	GX, GS, GT	0.82, 0.95	0.85, 1.0	0.88, 1.05	V
V_{CCT_GXBR} (2)	Transmitter analog power supply (right side)	GX, GS, GT	0.82, 0.95	0.85, 1.0	0.88, 1.05	V
V_{CCT_GTBR}	Transmitter analog power supply for GT channels (right side)	GT	0.95	1.0	1.05	V
V_{CCL_GTBR}	Transmitter clock network power supply	GT	0.95	1.0	1.05	V
V_{CCH_GXBL}	Transmitter output buffer power supply (left side)	GX, GS, GT	1.425	1.5	1.575	V
V_{CCH_GXBR}	Transmitter output buffer power supply (right side)	GX, GS, GT	1.425	1.5	1.575	V

Notes to Table 2–5:

(1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

(2) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 1.0 V or 0.85 V.

DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

Supply Current

Standby current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

I/O Pin Leakage Current

Table 2–6 lists the Stratix V I/O pin leakage current specifications.

Table 2–6. I/O Pin Leakage Current for Stratix V Devices—Preliminary

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–30	—	30	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–30	—	30	µA

Bus Hold Specifications

Table 2–7 lists the Stratix V device family bus hold specifications.

Table 2–7. Bus Hold Parameters for Stratix V Devices—Preliminary

Parameter	Symbol	Conditions	V_{CCIO}										Unit
			1.2 V		1.5 V		1.8 V		2.5 V		3.0 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (maximum)	22.5	—	25.0	—	30.0	—	50.0	—	70.0	—	µA
High sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (minimum)	–22.5	—	–25.0	—	–30.0	—	–50.0	—	–70.0	—	µA
Low overdrive current	I_{ODL}	$0V < V_{IN} < V_{CCIO}$	—	120	—	160	—	200	—	300	—	500	µA
High overdrive current	I_{ODH}	$0V < V_{IN} < V_{CCIO}$	—	–120	—	–160	—	–200	—	–300	—	–500	µA
Bus-hold trip point	V_{TRIP}	—	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 2–8 lists the Stratix V OCT termination calibration accuracy specifications.

Table 2–8. OCT Calibration Accuracy Specifications for Stratix V Devices—Preliminary (1) (Part 1 of 2)

Symbol	Description	Conditions	Calibration Accuracy			Unit
			C2	C3,I3	C4,I4	
25-Ω R_S	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	%
50-Ω R_S	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	%

Table 2–8. OCT Calibration Accuracy Specifications for Stratix V Devices—Preliminary (1) (Part 2 of 2)

Symbol	Description	Conditions	Calibration Accuracy			Unit
			C2	C3,I3	C4,I4	
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2 V	±15	±15	±15	%
48-Ω, 60-Ω, and 80-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, and 80-Ω setting)	V_{CCIO} = 1.2 V	±15	±15	±15	%
50-Ω R_T	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 2.5, 1.8, 1.5, 1.2 V	–10 to +40	–10 to +40	–10 to +40	%
20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25 V	–10 to +40	–10 to +40	–10 to +40	%
60-Ω and 120-Ω R_T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V_{CCIO} = 1.2	–10 to +40	–10 to +40	–10 to +40	%
25-Ω $R_{S\_left\_shift}$	Internal left shift series termination with calibration (25-Ω $R_{S\_left\_shift}$ setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	%

Note to Table 2–8:

(1) OCT calibration accuracy is valid at the time of calibration only.

Calibration accuracy for the calibrated series and parallel OCTs are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change. Table 2–9 lists the Stratix V OCT without calibration resistance tolerance to PVT changes.

Table 2–9. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices—Preliminary *(1)*

Symbol	Description	Conditions	Resistance Tolerance			Unit
			C2	C3, I3	C4, I4	
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.0 and 2.5 V	±30	±40	±40	%
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8 and 1.5 V	±30	±40	±40	%
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.2 V	±35	±50	±50	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.0 and 2.5 V	±30	±40	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8 and 1.5 V	±30	±40	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±35	±50	±50	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCIO} = 2.5 V	±25	±25	±25	%

Note to Table 2–9:

(1) Pending silicon characterization.

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 2–10 lists the OCT variation with temperature and voltage after power-up calibration. Use Table 2–10 to determine the OCT variation after power-up calibration and Equation 2–1 to determine the OCT variation without re-calibration.

Equation 2–1. OCT Variation Without Re-Calibration for Stratix V Devices—Preliminary *(1), (2), (3), (4), (5), (6)*

$$R_{OCT} = R_{SCAL}\left(1 + \langle\frac{dR}{dT} \times \Delta T\rangle \pm \langle\frac{dR}{dV} \times \Delta V\rangle\right)$$

Notes to Equation 2–1:

(1) The R_{OCT} value calculated from Equation 2–1 shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
(2) R_{SCAL} is the OCT resistance value at power-up.
(3) ΔT is the variation of temperature with respect to the temperature at power-up.
(4) ΔV is the variation of voltage with respect to the V_{CCIO} at power-up.
(5) dR/dT is the percentage change of R_{SCAL} with temperature.
(6) dR/dV is the percentage change of R_{SCAL} with voltage.

Table 2–10 lists the on-chip termination variation after power-up calibration.

Table 2–10. OCT Variation after Power-Up Calibration for Stratix V Devices—Preliminary *(1), (2)*

Symbol	Description	V_{CCIO} (V)	Typical	Unit
dR/dV	OCT variation with voltage without re-calibration	3.0	0.0297	%/mV
		2.5	0.0344	
		1.8	0.0499	
		1.5	0.0744	
		1.2	0.1241	
dR/dT	OCT variation with temperature without re-calibration	3.0	0.189	%/°C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.2	0.317	

Notes to Table 2–10:

(1) Valid for a V_{CCIO} range of ±5% and a temperature range of 0° to 85°C.
(2) Pending silicon characterization.

Pin Capacitance

Table 2–11 lists the Stratix V device family pin capacitance.

Table 2–11. Pin Capacitance for Stratix V Devices—Preliminary

Symbol	Description	Value	Unit
C_{IOTB}	Input capacitance on the top and bottom I/O pins	5.5	pF
C_{IOLR}	Input capacitance on the left and right I/O pins	5.5	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output and feedback pins	5.5	pF

Hot Socketing

Table 2–12 lists the hot socketing specifications for Stratix V devices.

Table 2–12. Hot Socketing Specifications for Stratix V Devices—Preliminary

Symbol	Description	Maximum
$I_{IOPIN\ (DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN\ (AC)}$	AC current per I/O pin	8 mA (1)
$I_{XCVR\text{-}TX\ (DC)}$ (2)	DC current per transceiver transmitter pin	100 mA
$I_{XCVR\text{-}RX\ (DC)}$ (2)	DC current per transceiver receiver pin	50 mA

Notes to Table 2–12:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C\ dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

(2) These specifications are preliminary.

Internal Weak Pull-Up Resistor

Table 2–13 lists the weak pull-up resistor values for Stratix V devices.

Table 2–13. Internal Weak Pull-Up Resistor for Stratix V Devices—Preliminary (1), (2)

Symbol	Description	V_{CCIO} Conditions (V) (3)	Value (4)	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option.	3.0 ±5%	25	kΩ
		2.5 ±5%	25	kΩ
		1.8 ±5%	25	kΩ
		1.5 ±5%	25	kΩ
		1.35 ±5%	25	kΩ
		1.25 ±5%	25	kΩ
		1.2 ±5%	25	kΩ

Notes to Table 2–13:

(1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.

(3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(4) These specifications are valid with a ±10% tolerance to cover changes over PVT.

I/O Standard Specifications

Table 2–14 through Table 2–19 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

For an explanation of the terms used in Table 2–14 through Table 2–19, refer to "Glossary" on page 2–32.

Table 2–14. Single-Ended I/O Standards for Stratix V Devices—Preliminary

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.6	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	–2

Table 2–15. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devices—Preliminary (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	0.49 * V_{CCIO}	0.5 * VCCIO	0.51 * V_{CCIO}
SSTL-135 Class I, II	1.283	1.35	1.418	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}
SSTL-125 Class I, II	1.19	1.25	1.26	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	0.49 * V_{CCIO}	0.5 * VCCIO	0.51 * V_{CCIO}
SSTL-12 Class I, II	1.14	1.20	1.26	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	0.49 * V_{CCIO}	0.5 * VCCIO	0.51 * V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—

Table 2–15. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devices—Preliminary (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 * V_{CCIO}	0.5 * V_{CCIO}	0.53 * V_{CCIO}	—	V_{CCIO}/2	—
HSUL-12	1.14	1.2	1.3	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	—	—	—

Table 2–16. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices—Preliminary (Part 1 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.608	V_{TT} + 0.608	8.1	–8.1
SSTL-2 Class II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
SSTL-18 Class I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	V_{TT} – 0.603	V_{TT} + 0.603	6.7	–6.7
SSTL-18 Class II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} – 0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 * V_{CCIO}	0.8 * V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 * V_{CCIO}	0.8 * V_{CCIO}	16	–16
SSTL-135 Class I, II	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	TBD (1)	TBD (1)	TBD (1)	TBD (1)
SSTL-125 Class I, II	—	V_{REF} – 0.85	V_{REF} + 0.85	—	V_{REF} – 0.15	V_{REF} + 0.15	TBD (1)	TBD (1)	TBD (1)	TBD (1)
SSTL-12 Class I, II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.15	V_{REF} + 0.15	TBD (1)	TBD (1)	TBD (1)	TBD (1)
HSTL-18 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25* V_{CCIO}	0.75* V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25* V_{CCIO}	0.75* V_{CCIO}	16	–16

Table 2–16. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices—Preliminary (Part 2 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1* V_{CCIO}	0.9* V_{CCIO}	TBD *(1)*	TBD *(1)*

Note to Table 2–16:

(1) Pending silicon characterization.

Table 2–17. Differential SSTL I/O Standards for Stratix V Devices—Preliminary

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)		$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.2	—	$V_{CCIO}/2$ + 0.2	0.62	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.15	—	$V_{CCIO}/2$ + 0.15
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.175	—	$V_{CCIO}/2$ + 0.175	0.5	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.125	—	$V_{CCIO}/2$ + 0.125
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	$V_{CCIO}/2$ – 0.15	—	$V_{CCIO}/2$ + 0.15	0.35	—	—	$V_{CCIO}/2$	—
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	—	V_{REF} –0.135	$V_{CCIO}/2$	V_{REF} + 0.135	TBD *(1)*	TBD *(1)*	V_{REF} –0.15	—	V_{REF} +0.15
SSTL-125 Class I, II	1.19	1.25	1.31	TBD *(1)*	—	TBD *(1)*	$V_{CCIO}/2$	TBD *(1)*	TBD *(1)*	—	TBD *(1)*	TBD *(1)*	TBD *(1)*
SSTL-12 Class I, II	1.14	1.2	1.26	TBD *(1)*	—	V_{REF} –0.15	$V_{CCIO}/2$	V_{REF} + 0.15	–0.30	0.30	TBD *(1)*	TBD *(1)*	TBD *(1)*

Note to Table 2–17:

(1) Pending silicon characterization.

Table 2–18. Differential HSTL and HSUL I/O Standards for Stratix V Devices—Preliminary

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO} + 0.3	—	0.5* V_{CCIO}	—	0.4* V_{CCIO}	0.5* V_{CCIO}	0.6* V_{CCIO}	0.3	V_{CCIO} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5*V_{CCIO} – 0.12	0.5* V_{CCIO}	0.5*V_{CCIO} + 0.12	0.4* V_{CCIO}	0.5* V_{CCIO}	0.6* V_{CCIO}	0.44	0.44

Table 2–19. Differential I/O Standard Specifications for Stratix V Devices—Preliminary *(1)*

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)			$V_{ICM(DC)}$ (V)			V_{OD} (V) *(2)*			V_{OCM} (V) *(2)*		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 2–20 on page 2–15.														
2.5 V LVDS	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	$D_{MAX} \leq$ 700 Mbps	1.8	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	D_{MAX} > 700 Mbps	1.55	0.247	—	0.6	1.125	1.25	1.375
BLVDS *(3)*	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—	—
RSDS (HIO)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO)	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL	2.375	2.5	2.625	300	—	—	0.6	$D_{MAX} \leq$ 700 Mbps	1.8 *(4)*	—	—	—	—	—	—
	2.375	2.5	2.625	300	—	—	1	D_{MAX} > 700 Mbps	1.6 *(4)*	—	—	—	—	—	—

Notes to Table 2–19:

(1) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 2–15.

(2) RL range: $90 \leq RL \leq 110\ \Omega$.

(3) There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. They depend on the system topology.

(4) For D_{MAX} > 700 Mbps, the minimum input voltage is 0.85 V; the maximum input voltage is 1.75 V. For $F_{MAX} \leq$ 700 Mbps, the minimum input voltage is 0.45 V; the maximum input voltage is 1.95 V.

Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus® II PowerPlay Power Analyzer feature.

You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as "Preliminary."
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 2–20 lists the Stratix V GX and GS transceiver specifications.

Table 2–20. Transceiver Specifications for Stratix V GX and GS Devices—Preliminary (1) (Part 1 of 4)

Symbol/ Description	Conditions	–1 Commercial Speed Grade			–2 Commercial/Industrial Speed Grade			–3 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL										
Input frequency from REFCLK input pins	—	40	—	710	40	—	710	40	—	710	MHz
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express® (PCIe®)	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—	0 to –0.5%	—	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	—	100	—	Ω
V_{ICM} (AC coupled)	—	1000/850 (2)			1000/850 (2)			1000/850 (2)			mV
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	250	—	550	mV
R_{REF}	—	—	2000 ±1%	—	—	2000 ±1%	—	—	2000 ±1%	—	Ω
Transceiver Clocks											
fixedclk clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	MHz

Table 2–20. Transceiver Specifications for Stratix V GX and GS Devices—Preliminary (1) (Part 2 of 4)

Symbol/ Description	Conditions	–1 Commercial Speed Grade			–2 Commercial/Industrial Speed Grade			–3 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Avalon-MM PHY management clock (phy_mgmt_clk) frequency	< 150										MHz
Reconfiguration clock (mgmt_clk_clk) frequency	—	100	—	125	100	—	125	100	—	125	MHz
Receiver											
Supported I/O Standards	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS										
Data rate (Standard PCS)	—	600	—	8500	600	—	8500	600	—	6500	Mbps
Data rate (10G PCS)	—	600	—	14100	600	—	12500	600	—	8500	Mbps
Absolute V_{MAX} for a receiver pin (3)	—	—	—	1.2	—	—	1.2	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	–0.4	—	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	V_{CCR_GXB} = 1.0 V	—	—	1.8	—	—	0.8	—	—	1.8	V
	V_{CCR_GXB} = 0.85 V	—	—	2.4	—	—	2.4	—	—	2.4	V
Minimum differential eye opening at receiver serial input pins (4)	—	85	—	—	85	—	—	85	—	—	mV
Differential on-chip termination resistors	85–Ω setting	85			85			85			Ω
	100–Ω setting	100			100			100			Ω
	120–Ω setting	120			120			120			Ω
	150-Ω setting	150			150			150			Ω
Programmable equalization (AC Gain)	Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz)	—	—	16	—	—	16	—	—	16	dB

Table 2–20. Transceiver Specifications for Stratix V GX and GS Devices—Preliminary (1) (Part 3 of 4)

Symbol/ Description	Conditions	–1 Commercial Speed Grade			–2 Commercial/Industrial Speed Grade			–3 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	2	—	—	2	—	—	2	—	dB
	DC Gain Setting = 2	—	4	—	—	4	—	—	4	—	dB
	DC Gain Setting = 3	—	6	—	—	6	—	—	6	—	dB
	DC Gain Setting = 4	—	8	—	—	8	—	—	8	—	dB
Transmitter											
Supported I/O Standards	1.4-V and 1.5-V PCML										
Data rate (Standard PCS)	—	600	—	8500	600	—	8500	600	—	6500	Mbps
Data rate (10G PCS)	—	600	—	14100	600	—	12500	600	—	8500	Mbps
V_{OCM}	0.65-V setting	—	650	—	—	650	—	—	650	—	mV
Differential on-chip termination resistors	85-Ω setting	85			85			85			Ω
	100-Ω setting	100			100			100			Ω
	120-Ω setting	120			120			120			Ω
	150-Ω setting	150			150			150			Ω
Rise time (5)	—	30	—	160	30	—	160	30	—	160	ps
Fall time (5)	—	30	—	160	30	—	160	30	—	160	ps
CMU PLL											
Supported Data Range	—	600	—	14100	600	—	12500	600	—	8500	Mbps
ATX PLL											
Supported Data Range	VCO post-divider L=1	8000	—	14100	8000	—	12500	8000	—	8500	Mbps
	L=2	4000	—	7050	4000	—	7050	4000	—	7050	Mbps
	L=4	2000	—	3525	2000	—	3525	2000	—	3525	Mbps
Input Reference Clock Frequency (6)	—	100	—	710	100	—	710	100	—	710	MHz

Table 2–20. Transceiver Specifications for Stratix V GX and GS Devices—Preliminary (1) (Part 4 of 4)

Symbol/ Description	Conditions	–1 Commercial Speed Grade			–2 Commercial/Industrial Speed Grade			–3 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transceiver-FPGA Fabric Interface											
Interface speed	—	25	—	283	25	—	266	25	—	250	MHz

Notes to Table 2–20:

(1) Speed grades shown in Table 2–20 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Family Overview* chapter.

(2) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.

(3) The device cannot tolerate prolonged operation at this absolute maximum.

(4) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(5) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

(6) The input reference clock frequency options depend on the data rate and the device speed grade.

Table 2–21 lists the Stratix V GT transceivers specifications.

Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 2–21 are the same as those listed in Table 2–20.

Table 2–21. Transceiver Specifications for Stratix V GT Devices—Preliminary

Symbol/ Description	Conditions	–2 Commercial/Industrial Speed Grade			–3 Commercial/Industrial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Clock								
V_{ICM} (AC coupled)	—	1000			1000			mV
Receiver								
Data rate (Standard PCS)	GX channels	600	—	8500	600	—	8500	Mbps
Data rate (10G PCS)	GX channels	600	—	12,500	600	—	12,500	Mbps
Data rate	GT channels	19,600	—	28,050	19,600	—	25,780	Mbps
Programmable equalization (AC Gain)	GT channels	—	15	—	—	15	—	dB
Differential on-chip termination resistors	GT channels	—	100	—	—	100	—	Ω
Transmitter								
Data rate (Standard PCS)	GX channels	600	—	8500	600	—	8500	Mbps
Data rate (10G PCS)	GX channels	600	—	12,500	600	—	12,500	Mbps
Data rate	GT channels	19,600	—	28,050	19,600	—	25,780	Mbps
Differential on-chip termination resistors	GT channels	—	100	—	—	100	—	Ω
Rise/Fall time	GT channels	—	15	—	—	15	—	ps

Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

Clock Tree Specifications

Table 2–22 lists the clock tree specifications for Stratix V devices.

Table 2–22. Clock Tree Performance for Stratix V Devices—Preliminary *(1)*

Performance				Unit
Symbol	–2 Speed Grade	–3 Speed Grade	–4 Speed Grade	
Global and Regional Clock	717	700	500	MHz
Periphery Clock	550	500	500	MHz

Note to Table 2–22:

(1) The Stratix V ES devices are limited for the 600 MHz core clock network frequency.

PLL Specifications

Table 2–23 lists the Stratix V PLL specifications when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (–40° to 100°C).

Table 2–23. PLL Specifications for Stratix V Devices—Preliminary *(1)* **(Part 1 of 3)**

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (–2 speed grade)	5	—	800 *(2)*	MHz
	Input clock frequency (–3 speed grade)	5	—	700 *(2)*	MHz
	Input clock frequency (–4 speed grade)	5	—	650 *(2)*	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{FINPFD}	Fractional Input clock frequency to the PFD	50	—	133	MHz
f_{VCO}	PLL VCO operating range (–2 speed grade)	600	—	1600	MHz
	PLL VCO operating range (–3 speed grade)	600	—	1400	MHz
	PLL VCO operating range (–4 speed grade)	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%
f_{OUT}	Output frequency for an internal global or regional clock (–2 speed grade)	—	—	717 *(3)*	MHz
	Output frequency for an internal global or regional clock (–3 speed grade)	—	—	700 *(3)*	MHz
	Output frequency for an internal global or regional clock (–4 speed grade)	—	—	500 *(3)*	MHz
f_{OUT_EXT}	Output frequency for an external clock output (–2 speed grade)	—	—	800 *(3)*	MHz
	Output frequency for an external clock output (–3 speed grade)	—	—	667 *(3)*	MHz
	Output frequency for an external clock output (–4 speed grade)	—	—	533 *(3)*	MHz

Table 2–23. PLL Specifications for Stratix V Devices—Preliminary (1) (Part 2 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{OUTDUTY}$	Duty cycle for an external clock output (when set to **50%**)	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	10	ns
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift	—	TBD (1)	—	—
$f_{DYCONFIGCLK}$	Dynamic Configuration Clock	—	—	100	MHz
t_{LOCK}	Time required to lock from the end-of-device configuration or deassertion of `areset`	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth (8)	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the `areset` signal	10	—	—	ns
t_{INCCJ} (4), (5)	Input clock cycle-to-cycle jitter ($f_{REF} \geq 100$ MHz)	—	0.15	—	UI (p-p)
	Input clock cycle-to-cycle jitter ($f_{REF} < 100$ MHz)	–750	—	+750	ps (p-p)
t_{OUTPJ_DC} (6)	Period Jitter for dedicated clock output ($f_{OUT} \geq 100$ MHz)	—	—	TBD (1)	ps (p-p)
	Period Jitter for dedicated clock output ($f_{OUT} < 100$ MHz)	—	—	TBD (1)	mUI (p-p)
t_{OUTCCJ_DC} (6)	Cycle-to-Cycle Jitter for a dedicated clock output ($f_{OUT} \geq 100$ MHz)	—	—	TBD (1)	ps (p-p)
	Cycle-to-Cycle Jitter for a dedicated clock output ($f_{OUT} < 100$ MHz)	—	—	TBD (1)	mUI (p-p)
t_{OUTPJ_IO} (6), (9)	Period Jitter for a clock output on a regular I/O ($f_{OUT} \geq 100$ MHz)	—	—	TBD (1)	ps (p-p)
	Period Jitter for a clock output on a regular I/O ($f_{OUT} < 100$ MHz)	—	—	TBD (1)	mUI (p-p)
t_{OUTCCJ_IO} (6), (9)	Cycle-to-Cycle Jitter for a clock output on a regular I/O ($f_{OUT} \geq 100$ MHz)	—	—	TBD (1)	ps (p-p)
	Cycle-to-Cycle Jitter for a clock output on a regular I/O ($f_{OUT} < 100$ MHz)	—	—	TBD (1)	mUI (p-p)
$t_{CASC\_OUTPJ\_DC}$ (6), (7)	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} \geq 100$ MHz)	—	—	TBD (1)	ps (p-p)
	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} < 100$ MHz)	—	—	TBD (1)	mUI (p-p)
f_{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 µs	—	—	±10	%
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	24	—	Bits
k_{VALUE}	Numerator of Fraction	—	8388608	—	—

Table 2–23. PLL Specifications for Stratix V Devices—Preliminary (1) (Part 3 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
f_{RES}	Resolution of VCO frequency (f_{INPFD} = 100 MHz)	—	5.96	—	Hz

Notes to Table 2–23:

(1) Pending silicon characterization.

(2) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(3) This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.

(4) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.

(5) f_{REF} is fIN/N when N = 1.

(6) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 2–36 on page 2–30.

(7) The cascaded PLL specification is only applicable with the following condition:
a. Upstream PLL: 0.59Mhz ≤ Upstream PLL BW < 1 MHz
b. Downstream PLL: Downstream PLL BW > 2 MHz

(8) High bandwidth PLL settings are not supported in external feedback mode.

(9) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 2–34 on page 2–29.

DSP Block Specifications

Table 2–24 lists the Stratix V DSP block performance specifications.

Table 2–24. Block Performance Specifications for Stratix V DSP Devices—Preliminary (1) (Part 1 of 2)

Mode	Performance			Unit
	–2 Speed Grade	–3 Speed Grade	–4 Speed Grade	
Modes using One DSP				
Three 9 × 9	600	480	420	MHz
One 18 × 18	600	480	420	MHz
Two partial 18 × 18 (or 16 × 16)	600	480	420	MHz
One 27 × 27	450	360	315	MHz
One 36 × 18	450	360	315	MHz
One sum of two 18 × 18 (One sum of two 16 × 16)	500	400	350	MHz
One sum of square	450	360	315	MHz
One 18 × 18 plus 36 (a × b) + c	500	400	350	MHz
Modes using Two DSPs				
Three 18 × 18	500	400	350	MHz
One sum of four 18 × 18	425	340	298	MHz
One sum of two 27 × 27	425	340	298	MHz
One sum of two 36 × 18	425	340	298	MHz
One complex 18 × 18	500	400	350	MHz
One 36 × 36	400	320	280	MHz
Modes using Three DSPs				
One complex 18 × 25	350	280	245	MHz

Table 2–24. Block Performance Specifications for Stratix V DSP Devices—Preliminary (1) (Part 2 of 2)

Mode	Performance			Unit
	–2 Speed Grade	–3 Speed Grade	–4 Speed Grade	
Modes using Four DSPs				
One complex 27 × 27	425	340	298	MHz

Note to Table 2–24:

(1) These numbers are preliminary pending silicon characterization.

Memory Block Specifications

Table 2–25 lists the Stratix V memory block specifications.

Table 2–25. Memory Block Performance Specifications for Stratix V Devices—Preliminary (1), (2), (3)

Memory	Mode	Resources Used		Performance					Unit
		ALUTs	Memory	C2 Speed Grade	C3 Speed Grade	I3 Speed Grade	C4 Speed Grade	I4 Speed Grade	
MLAB	Single port, all supported widths	0	1	600	500	500	450	450	MHz
	Simple dual-port, x32/x64 width	0	1	450	400	TBD	315	TBD	MHz
	Simple dual-port, x16 width	0	1	675	533	533	400	400	MHz
	ROM, all supported widths	0	1	600	500	500	450	450	MHz
M20K Block	Single-port, all supported widths	0	1	700	650	500	550	450	MHz
	Simple dual-port, all supported widths	0	1	700	650	500	550	450	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	0	1	525	455	455	400	400	MHz
	Simple dual-port with ECC enabled, 512 × 32	0	1	450	400	400	350	350	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	0	1	600	500	500	450	450	MHz
	True dual port, all supported widths	0	1	700	650	500	550	450	MHz
	ROM, all supported widths	0	1	700	650	500	550	450	MHz
	Min Pulse Width (clock high time)	—	—	750	800	800	850	850	ps
	Min Pulse Width (clock low time)	—	—	500	625	625	690	690	ps

Notes to Table 2–25:

(1) These numbers are preliminary pending silicon characterization.

(2) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(3) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.

JTAG Configuration Specifications

Table 2–26 lists the JTAG timing parameters and values for Stratix V devices.

Table 2–26. JTAG Timing Parameters and Values for Stratix V Devices—Preliminary *(1)*

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11 *(2)*	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 *(2)*	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 *(2)*	ns

Notes to Table 2–26:

(1) These numbers are preliminary pending silicon characterization.

(2) A 1 ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, t_{JPCO} = 12 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

Temperature Sensing Diode Specifications

Table 2–27 lists the specifications for the Stratix V temperature sensing diode.

Table 2–27. External Temperature Sensing Diode Specifications for Stratix V Devices—Preliminary

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	8	—	200	µA
$V_{bias,}$ voltage across diode	0.3	—	0.9	V
Series resistance	—	—	< 1	Ω
Diode ideality factor	—	—	1.01	—

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

The actual achievable frequency depends on design- and system-specific factors. You must perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 2–28 lists high-speed I/O timing for Stratix V devices.

Table 2–28. High-Speed I/O Specifications for Stratix V Devices—Preliminary (1), (2), (3) (Part 1 of 2)

Symbol	Conditions	–2 Speed Grade			–3 Speed Grade			–4 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 (5)	5	—	717	5	—	625	5	—	525	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards (4)	Clock boost factor W = 1 to 40 (5)	5	—	717	5	—	625	5	—	525	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards (3)	Clock boost factor W = 1 to 40 (5)	5	—	520	5	—	420	5	—	420	MHz
f_{HSCLK_OUT} (output clock frequency)	—	5	—	717 (6)	5	—	625 (6)	5	—	525 (6)	MHz
Transmitter											
True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J = 3 to 10 (10)	(7)	—	1434	(7)	—	1250	(7)	—	1050	Mbps
	SERDES factor J = 2, uses DDR Registers	(7)	—	(7)	(7)	—	(7)	(7)	—	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(7)	—	(7)	(7)	—	(7)	(7)	—	(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f_{HSDR} (data rate) (8)	SERDES factor J = 4 to 10	(7)	—	1100	(7)	—	840	(7)	—	840	Mbps
$t_{x\ Jitter}$ - True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	UI
$t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	300	—	—	300	—	—	325	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.2	—	—	0.2	—	—	0.25	UI
t_{DUTY}	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	%

Table 2–28. High-Speed I/O Specifications for Stratix V Devices—Preliminary (1), (2), (3) (Part 2 of 2)

Symbol	Conditions	–2 Speed Grade			–3 Speed Grade			–4 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{RISE} & t_{FALL}	True Differential I/O Standards	—	—	160	—	—	200	—	—	200	ps
	Emulated Differential I/O Standards with three external output resistor networks	—	—	250	—	—	250	—	—	300	ps
TCCS	True Differential I/O Standards	—	—	150	—	—	150	—	—	150	ps
	Emulated Differential I/O Standards	—	—	300	—	—	300	—	—	300	ps
Receiver											
True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 3 to 10	150	—	1434	150	—	1250	150	—	1050	Mbps
f_{HSDR} (data rate)	SERDES factor J = 3 to 10	(7)	—	(9)	(7)	—	(9)	(7)	—	(9)	Mbps
	SERDES factor J = 2, uses DDR Registers	(7)	—	(7)	(7)	—	(7)	(7)	—	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(7)	—	(7)	(7)	—	(7)	(7)	—	(7)	Mbps
DPA Mode											
DPA run length	—	—	—	10000	—	—	10000	—	—	10000	UI
Soft CDR mode											
Soft-CDR PPM tolerance	—	—	—	300	—	—	300	—	—	300	± PPM
Non DPA Mode											
Sampling Window	—	—	—	300	—	—	300	—	—	300	ps

Notes to Table 2–28:

(1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.

(2) When J = 1 or 2, bypass the SERDES block.

(3) This only applies to **LVDS** source synchronous mode.

(4) This only applies to DPA and soft-CDR modes.

(5) Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.

(6) This is achieved by using the **LVDS** clock network.

(7) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(8) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

(9) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

(10) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

Figure 2–1 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 2–1. DPA Lock Time Specification with DPA PLL Calibration Enabled

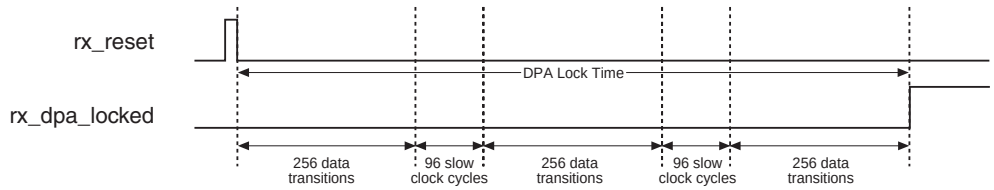


Table 2–29 lists the DPA lock time specifications for Stratix V GX devices.

Table 2–29. DPA Lock Time Specifications for Stratix V GX Devices Only—Preliminary *(1), (2), (3)*

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions *(4)*	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
	01010101	8	32	640 data transitions

Notes to Table 2–29:

(1) The DPA lock time is for one channel.
(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
(3) The DPA lock time stated in this table applies to both commercial and industrial grade.
(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 2–2 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps. Table 2–30 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps.

Figure 2–2. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate ≥ 1.25 Gbps

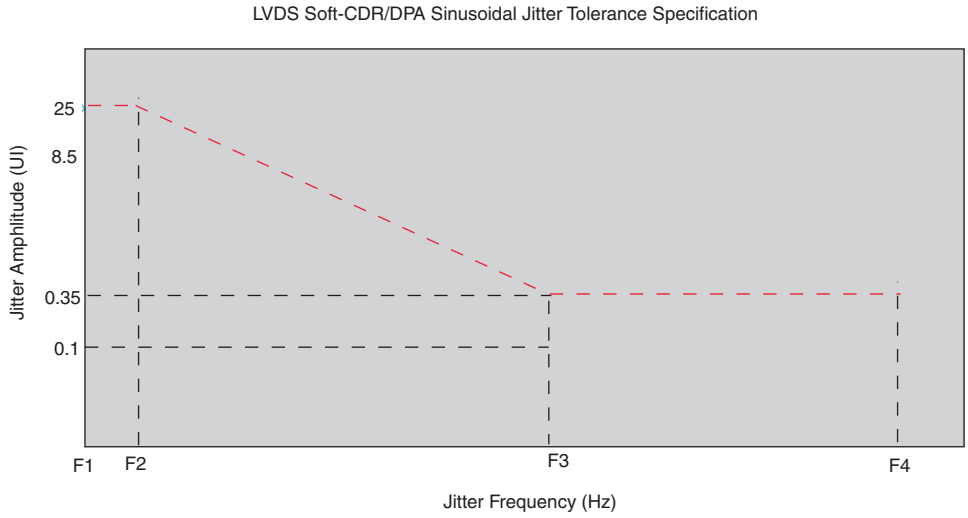
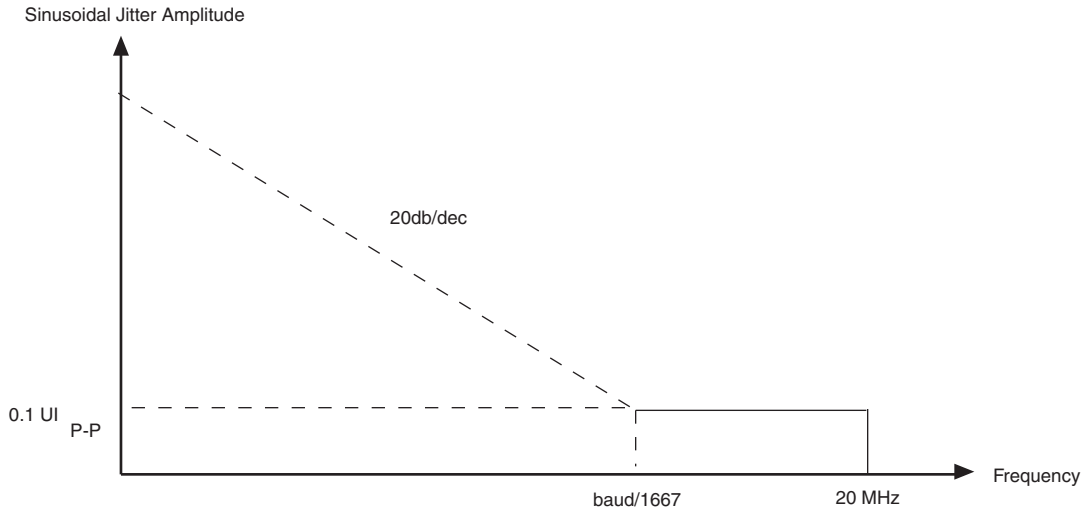


Table 2–30. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate ≥ 1.25 Gbps—Preliminary

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Figure 2–3 shows the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate < 1.25 Gbps.

Figure 2–3. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate < 1.25 Gbps



DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 2–31 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

Table 2–31. DLL Range Specifications for Stratix V Devices *(1)*

–2 Speed Grade	–3 Speed Grade	–4 Speed Grade	Unit
300-1120	300-890	300-890	MHz

Note to Table 2–31:

(1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 2–32 lists the DQS phase offset delay per stage for Stratix V devices.

Table 2–32. DQS Phase Offset Delay Per Setting for Stratix V Devices—Preliminary *(1), (2), (3)*

Speed Grade	Min	Max	Unit
–2	7	13	ps
–3	7	15	ps
–4	7	16	ps

Notes to Table 2–32:

(1) These numbers are preliminary pending silicon characterization.

(2) The typical value equals the average of the minimum and maximum values.

(3) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a –2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10 ps) ± 20 ps] = 725 ps ± 20 ps.

Table 2–33 lists the DQS phase shift error for Stratix V devices.

Table 2–33. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Stratix V Devices—Preliminary *(1), (2)*

Number of DQS Delay Buffers	–2 Speed Grade	–3 Speed Grade	–4 Speed Grade	Unit
1	26	28	30	ps
2	52	56	60	ps
3	78	84	90	ps
4	104	112	120	ps

Notes to Table 2–33:

(1) The numbers are preliminary pending silicon characterization.

(2) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a –2 speed grade is ±78 ps or ±39 ps.

Table 2–34 lists the memory output clock jitter specifications for Stratix V devices.

Table 2–34. Memory Output Clock Jitter Specification for Stratix V Devices *(1)*

Clock Network	Parameter	Symbol	–2 Speed Grade		–3 Speed Grade		–4 Speed Grade		Unit
			Min	Max	Min	Max	Min	Max	
Regional	Clock period jitter	$t_{JIT(per)}$	–50	50	–55	55	–55	55	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–100	100	–110	110	–110	110	ps
	Duty cycle jitter	$t_{JIT(duty)}$	–50	50	–82.5	82.5	–82.5	82.5	ps
Global	Clock period jitter	$t_{JIT(per)}$	–75	75	–82.5	82.5	–82.5	82.5	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–150	150	–165	165	–165	165	ps
	Duty cycle jitter	$t_{JIT(duty)}$	–75	75	–90	90	–90	90	ps
PHY Clock	Clock period jitter	$t_{JIT(per)}$	–25	25	–30	30	–35	35	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–50	50	–60	60	–70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	–37.5	37.5	–45	45	–56	56	ps

Note to Table 2–34:

(1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

OCT Calibration Block Specifications

Table 2–35 lists the OCT calibration block specifications for Stratix V devices.

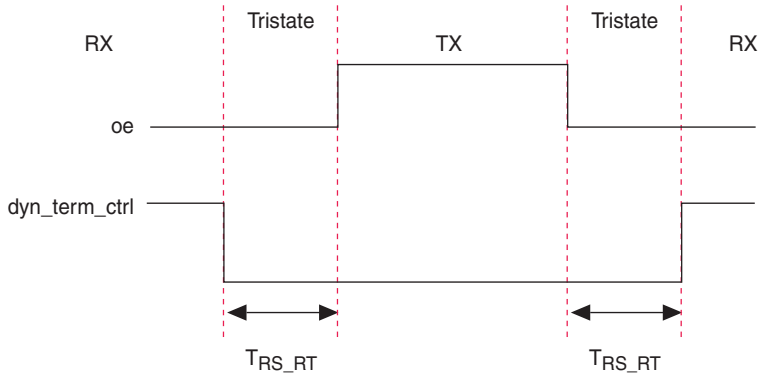
Table 2–35. OCT Calibration Block Specifications for Stratix V Devices—Preliminary *(1)*

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT R_S/R_T calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R_S and R_T (Figure 2–4)	—	2.5	—	ns

Note to Table 2–35:

(1) Pending silicon characterization.

Figure 2–4. Timing Diagram for oe and dyn_term_ctrl Signals



Duty Cycle Distortion (DCD) Specifications

Table 2–36 lists the worst-case DCD for Stratix V devices.

Table 2–36. Worst-Case DCD on Stratix V I/O Pins—Preliminary *(1)*

Symbol	–2 Speed Grade		–3 Speed Grade		–4 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	%

Note to Table 2–36:

(1) The numbers are preliminary pending silicon characterization.

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Literature webpage.

Programmable IOE Delay

Table 2–37 lists the Stratix V IOE programmable delay settings.

Table 2–37. IOE Programmable Delay for Stratix V Devices—Preliminary *(1)*

Parameter *(2)*	Available Settings	Min Offset *(3)*	Fast Model		Slow Model					
			Industrial	Commercial	C2	C3	C4	I3	I4	Unit
D1	63	0	0.471	0.514	0.800	0.843	0.918	0.850	0.924	ns
D2	31	0	0.274	0.274	0.423	0.456	0.501	0.453	0.498	ns
D3	7	0	1.668	1.735	2.830	2.985	3.252	3.007	3.274	ns
D5	63	0	0.493	0.474	0.835	0.882	0.960	0.888	0.966	ns
D6	31	0	0.273	0.258	0.463	0.488	0.532	0.492	0.536	ns

Notes to Table 2–37:

(1) Pending the Quartus II software extraction.
(2) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**,**D5**, and **D6** in the **Assignment Name** column.
(3) Minimum offset does not include the intrinsic delay.

Programmable Output Buffer Delay

Table 2–38 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Table 2–38. Programmable Output Buffer Delay for Stratix V Devices—Preliminary *(1)*, *(2)*

Symbol	Parameter	Typical	Unit
D_{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

Notes to Table 2–38:

(1) Pending the Quartus II software extraction.
(2) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

Glossary

Table 2–39 lists the glossary for this chapter.

Table 2–39. Glossary (Part 1 of 4)

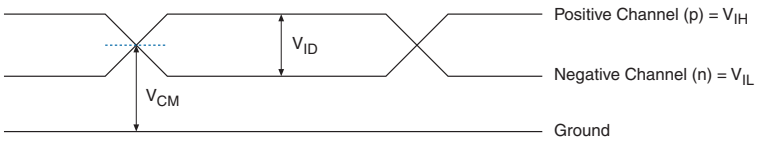
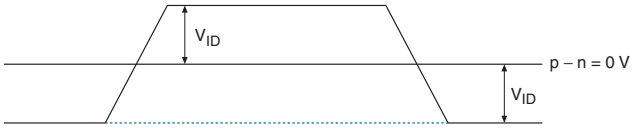
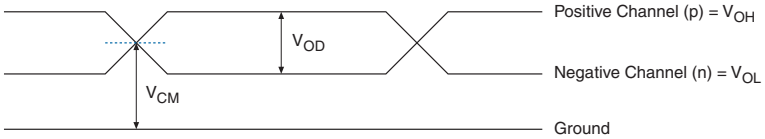
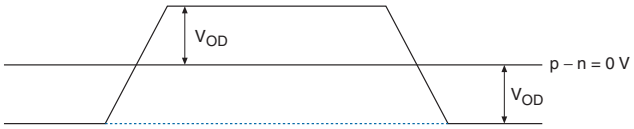
Letter	Subject	Definitions
A B C	—	—
D	Differential I/O Standards	*Receiver Input Waveforms* **Single-Ended Waveform**  **Differential Waveform**  *Transmitter Output Waveforms* **Single-Ended Waveform**  **Differential Waveform** 
E	—	—
F	f_{HSCLK}	Left and right PLL input clock frequency.
	f_{HSDR}	High-speed I/O block—Maximum and minimum **LVDS** data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
	$f_{HSDRDPA}$	High-speed I/O block—Maximum and minimum **LVDS** data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
G H I	—	—

Table 2–39. Glossary (Part 2 of 4)

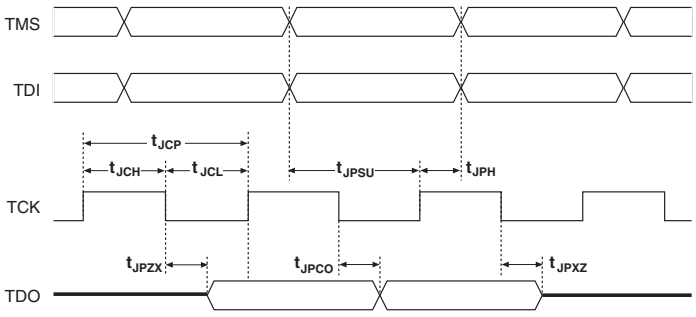
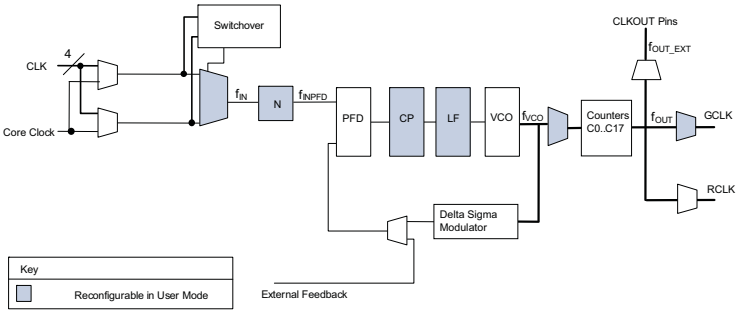
Letter	Subject	Definitions
J	J	High-speed I/O block—Deserialization factor (width of parallel data bus).
	JTAG Timing Specifications	JTAG Timing Specifications: 
K **L** **M** **N** **O**	—	—
P	**PLL Specifications**	**Diagram of PLL Specifications** *(1)*  **Note:** (1) `Core Clock` can only be fed by dedicated clock input pins or PLL outputs.
Q	—	—
R	R_L	Receiver differential input discrete resistor (external to the Stratix V device).

Table 2–39. Glossary (Part 3 of 4)

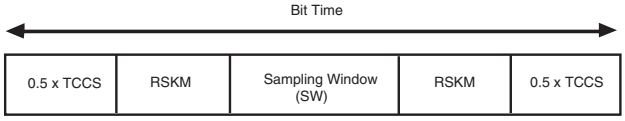
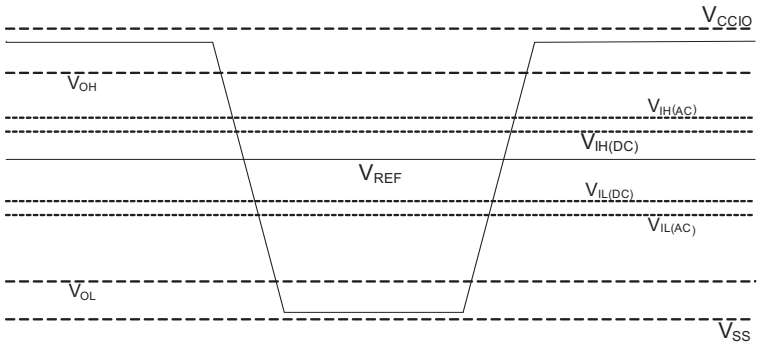
Letter	Subject	Definitions
S	**SW (sampling window)**	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown: 
	Single-ended voltage referenced I/O standard	The JEDEC standard for **SSTI** and **HSTL** I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the AC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing, as shown: *Single-Ended Voltage Referenced I/O Standard* 
T	t_C	High-speed receiver and transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the *Timing Diagram* figure under **SW** in this table).
	t_{DUTY}	High-speed I/O block—Duty cycle on the high-speed transmitter output clock.
		Timing Unit Interval (TUI) The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(receiver input clock frequency multiplication factor) = t_C/w)
	t_{FALL}	Signal high-to-low transition time (80-20%)
	t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.
	t_{OUTPJ_IO}	Period jitter on the general purpose I/O driven by a PLL.
	t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL.
	t_{RISE}	Signal low-to-high transition time (20-80%)
U	—	—

Table 2–39. Glossary (Part 4 of 4)

Letter	Subject	Definitions
V	$V_{CM(DC)}$	DC common mode input voltage.
	V_{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	V_{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V_{SWING}	Differential input voltage
	V_X	Input differential cross point voltage
	V_{OX}	Output differential cross point voltage
W	W	High-speed I/O block—clock boost factor
X Y Z	—	—

Document Revision History

Table 2–40 lists the revision history for this chapter.

Table 2–40. Document Revision History (Part 1 of 2)

Date	Version	Changes
December 2011	2.2	■ Added Table 2–31. ■ Updated Table 2–28 and Table 2–34.
November 2011	2.1	■ Added Table 2–2 and Table 2–21 and updated Table 2–5 with information about Stratix V GT devices. ■ Updated Table 2–11, Table 2–13, Table 2–20, and Table 2–25. ■ Various edits throughout to fix SPRs.

Table 2–40. Document Revision History (Part 2 of 2)

Date	Version	Changes
May 2011	2.0	■ Updated Table 2–4, Table 2–18, Table 2–19, Table 2–21, Table 2–22, Table 2–23, and Table 2–24. ■ Updated the "DQ Logic Block and Memory Output Clock Jitter Specifications" title. ■ Chapter moved to Volume 1. ■ Minor text edits.
December 2010	1.1	■ Updated Table 1–2, Table 1–4, Table 1–19, and Table 1–23. ■ Converted chapter to the new template. ■ Minor text edits.
July 2010	1.0	Initial release.

This chapter provides additional information about the document and Altera.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
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	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general)	Email	nacomp@altera.com
(software licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."

Visual Cue	Meaning
Courier type	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	The question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	The multimedia icon directs you to a related multimedia presentation.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.